A Broadband 800 GHz Schottky Balanced Doubler

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***Abstract*—A broadband planar Schottky balanced doubler at 800 GHz has been designed and built. The design utilizes two Schottky diodes in a balanced configuration on a 12 μm thick Gallium Arsenide (GaAs) substrate as a supporting frame. This broadband doubler (designed for 735 GHz to 850 GHz) uses a split waveguide block and has a relatively simple, fast, and robust assembly procedure. The doubler achieved $\approx$ 10% efficiency at 765 GHz, giving 1.1 mW of peak output power when pumped with about 9 mW of input power at room temperature.**

***Index Terms*—Balanced doubler, broadband, millimeter waves, Schottky diode.**

I. Introduction

MILLIMETER and submillimeter wave detectors for astronomical, remote sensing, and atmospheric sciences applications are being developed with ever-increasing capability to meet the growing demands of the immensely powerful set of new and future space-borne and ground-based telescopes and facilities. Many of these instruments have cryogenically-cooled heterodyne receivers, which use superconductor insulator superconductor (SIS) and hot electron bolometer (HEB) mixers for use in high sensitivity, high resolution spectroscopy measurements. These receivers require wideband fixed-tuned local oscillator (LO) sources which are robust, easy to implement, cryogenically cool-able, and reliable.

Current state-of-the-art solid state sources above 200 GHz are constructed from chains of cascaded Schottky-barrier varactor diode frequency multipliers. Using a new planar substrateless technology [1], we have designed and developed an 800 GHz broadband doubler for use in the 735 GHz to 850 GHz frequency range. This balanced doubler incorporates a pair of diodes configured symmetrically so that they only respond to odd harmonics at the input and even harmonics at the output, making it easier to separate the input and output frequencies without any filter structures [2]. The balanced design also facilitates broadband operation by eliminating the need to incorporate frequency filtering within the impedance matching circuitry.

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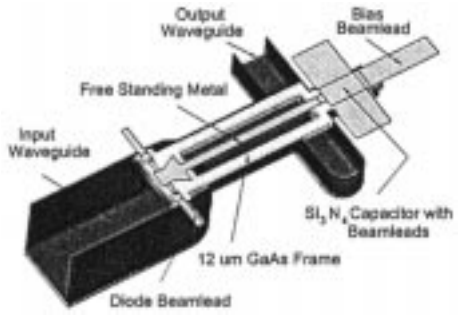

Fig. 1. Sketch of an 800 GHz doubler. The doubler chip rests on its beam leads on the split waveguide block. The diodes are operated under reverse bias condition and are biased through the bias beam lead.

II. Design, Fabrication, and Assembly

The 800 GHz balanced doubler design process involves a few steps: Advanced Design System's (ADS) [3] nonlinear harmonic balance simulator, in conjunction with our Schottky varactor diode model [4], is used to optimize the doping profile and diode dimensions such as the anode and mesa size for a given input power (we used 7 mW input power for our design). From this simulation, we also calculate the diode junction characteristics as a function of frequency and the embedding impedances for optimum performance of the multiplier. Then, the multiplier input and output matching circuits are synthesized using high frequency structure simulator (HFSS)—a finite element electromagnetic simulator [5]. Using the S-parameters obtained from HFSS simulations and the diode properties obtained from the nonlinear diode simulations, we optimize the design in a linear simulator with waveguide matching components for maximum doubler efficiency. Finally, we put all the components in the nonlinear harmonic balance simulator which predicts the performance of the doubler.

The input signal is directly coupled to the diodes which are placed in a reduced height input waveguide. The output signal is coupled to the output waveguide by means of an E-field probe. The input matching is accomplished with the input backshort and waveguide matching sections and the output circuit is optimized using waveguide matching components, a waveguide channel connecting the input and output waveguides and a small open stub on the input side of the diode which tunes out the excess inductance of the diode structure at the output frequency. An integrated silicon nitride (Si_3N_4) capacitor, at the end of the output coupling probe, is used as RF short and dc bypass. One of the critical design criteria is to make the input reduced height section below cut-off for TM_{11} mode at the output frequency. The cavity for the integrated capacitor should also be designed carefully not to allow any output frequency signal to leak through it. This design methodology does not necessarily

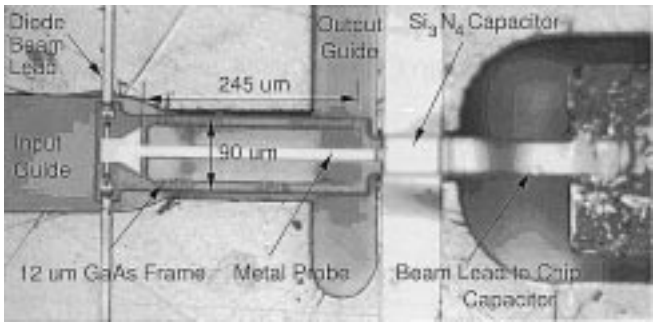

Fig. 2. Picture of an assembled 800 GHz doubler.

lead to a single implementation when it comes to the chip technology and topography. A number of implementation choices can be made which are based on practical concerns such as chip handling, sensitivity to dimensional tolerances, and circuit assembly issues to name a few. We have designed a number of slightly different circuit variations to cover most of the concerns. Fig. 1 shows the sketch of one such doubler chip placed inside the split waveguide block.

The device and circuitry for the doubler is fabricated on a Gallium Arsenide (GaAs) substrate using optical lithography [6]. What is unique about this fabrication process is the use of metal beam leads for dc and RF contacts with waveguides. Also, to minimize dielectric loading of the waveguides and to reduce RF losses in passive circuit elements, the GaAs substrate under the transmission lines is removed in back-side processing, leaving free standing metal lines suspe nded in air from a nominally 12 μm thick GaAs frame.

Assembly for this device is relatively simple, fast, and robust. The diode chip is dropped inside the split waveguide block with the diode beam leads resting on the waveguide metal. The beam lead from the integrated capacitor is bonded to a chip capacitor, which, in turn, is wire-bonded to the bias connector. There is no soldering or other high temperature procedure used on the device and that reduces the possibility of device damage. The picture of an assembled doubler is shown in Fig. 2.

III. Measurement and Results

Initial measurements for the doubler are carried out at room temperature using a wideband calorimeter [7]. A pump source generates a signal in the 90–110 GHz frequency range, which is amplified and power combined to generate about 200 mW of input power. This signal is used to drive our 200 GHz and 400 GHz doublers [1] to generate about 7 mW of pump signal across a reasonable bandwidth for the 800 GHz doubler. The anode size for the diode used for this measurement is $1.1\,\mu\text{m} \times 1.0\,\mu\text{m}$ and has $4 \times 10^{17}/\text{cm}^3$ epitaxial layer doping, giving a zero-bias capacitance (C_{j0}) of about 2.7 fF. The performance of the doubler at room temperature is shown in Fig. 3. For this measurement, output power was measured quasioptically using a Thomas Keating power meter [8]. The result shown does not correct for any losses in the circuits, the waveguides, or any other external components. We measured about 1.1 mW of peak output power at room temperature at 765 GHz when pumped with about 9 mW of input power. From this, the efficiency was calculated to be more than 10% at this frequency. It can be seen from Fig. 3 that the output power more or less follows the input pump power.

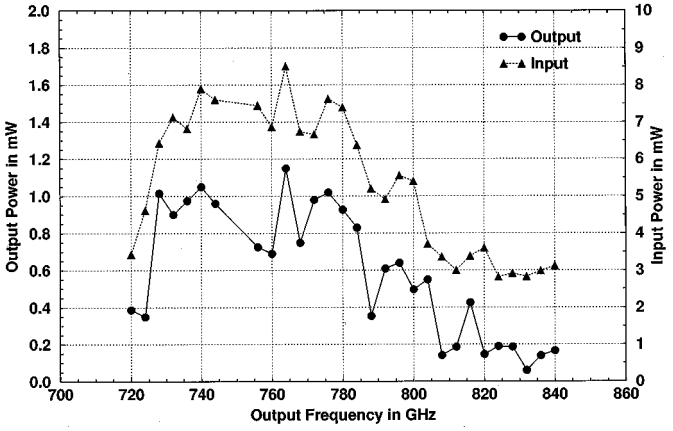

Fig. 3. Performance of the doubler at room temperature. The dotted line shows the input power used to pump the doubler. For this measurement, the diodes were optimally biased at each and every frequency points and the bias voltage range used was from -1 volt to -3 volts.

IV. Conclusion

We have designed, fabricated, and partly evaluated the first-ever planar Schottky diode doubler around 800 GHz. The peak output power from this doubler when pumped with existing planar Schottky diode multipliers puts out more than 1 mW at room temperature. This work leads us to make two important conclusions. First, current planar design and device technology are sufficient to provide fixed-tuned broadband doublers in the 800 GHz range and, second, these stages can now provide enough output power to enable sufficient pumping of the next stage multipliers, i.e., 1600 GHz doublers and 2400 GHz triplers.

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